REMARKS

Claims 1-11 are pending in the present application. Claim 1, 2, 3, 4 and 7 have been amended in this response. Favorable reconsideration is respectfully requested in view of the remarks presented herein below.

Claim Objections

Claim 3 is objected to under 37 CFR 1.75 (c) as being in improper form because a multiple dependent claims should refer to other claims in the alternative only. Claim 3 has been amended to overcome the objection. Withdrawal of the objection is respectfully requested.

Claim Rejections Under 35 U.S.C. §112

Claims 1, 2, 5 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. This rejection is respectfully traversed.

The Examiner contends that the recitation of a "recording medium" in claims 1, 2, 5 and 8 is not clearly defined in the specification and thus, the scope of the claims is not ascertainable in view of the specification. However, contrary to the assertion by the Examiner, examples of a recording medium are clearly disclosed in the specification. See lines 24-26, page 15 of the specification. Thus, claims 1, 2, 5 and 8 are definite and it is respectfully submitted that this rejection should be withdrawn.

Claim Rejections Under 35 U.S.C. §103

Claims 1, 2 and 4-11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,907,275 to Hashimoto (hereinafter "Hashimoto") in view of U.S. Patent No. 5,392,351 to Hasebe, et al. (hereinafter "Hasebe"). This rejection is respectfully traversed.

Independent claim 1 as amended recites, *inter alia*, "the encryption circuit being deactivated before the data control circuit receives the digital recording signal to be encrypted ...wherein when the digital recording signal needs to be encrypted, the encryption circuit begins to start up and the digital recording signal is transmitted from the data control circuit to the

memory to be stored in the memory during start-up of the encryption circuit, and when the encryption circuit becomes capable of operation, the digital recording signal stored in the memory is transmitted via the data control circuit to the encryption circuit and is encrypted by the encryption circuit to be recorded in the recording unit."

Hashimoto describes an encryption apparatus, in which, prior to encryption process, information indicating whether plain text blocks are to be encrypted or not is stored in a mask register. In the encryption process, only the plain text blocks to be encrypted are read from an input buffer, encrypted by an encryption circuit, and stored in an output buffer. The plain text blocks not to be encrypted are sequentially read from the input buffer in the ascending order of the addresses and they are stored, without being encrypted, in the output buffer at the corresponding addresses to the input buffer addresses at which the plain text blocks have been stored. See Abstract of Hashimoto. In contrast, the present invention provides an encryption circuit that is deactivated before the data control circuit receives the digital recording signal to be encrypted. Furthermore, when a digital recording signal needs to be encrypted, an encryption circuit begins to start up and the digital recording signal is transmitted from the data control circuit to the memory to be stored in the memory during start-up of the encryption circuit and when the encryption circuit becomes capable of operation, the digital recording signal stored in the memory is transmitted via the data control circuit to the encryption circuit and is encrypted by the encryption circuit to be recorded in the recording unit as in claim 1. Hashimoto does not disclose or suggest these features.

The Examiner contends that the purpose of a buffer is to store data after it is transferred but before it can be processed either due to the circuit not having complete start-up or it is currently processing other data. However, Hashimoto merely describes an encryption processor that encrypts data of an input buffer and stores it into an output buffer. Contrary to the Examiner's assertion, nowhere in Hashimoto is there a disclosure or suggestion of a buffer having a purpose of storing data due to the circuit not having complete start-up. The present invention seeks to provide a recording/reproducing unit that enables an encryption/decryption circuit only when encryption/decryption is required without interrupting recording/reproducing. Specifically, data can be continuously recorded/reproduced during a period of time from a time

when a program that does not need to be encrypted/decrypted is switched to a program that needs to be encrypted/decrypted to a time when the recording/reproducing unit is ready to record an encrypted/decrypted signal. On the other hand, Hashimoto is not concerned with providing such features. Furthermore, the Examiner's reasoning for supporting the rejection appears to be based on impermissible hindsight. *See MPEP 2141.* Thus, if this rejection is maintained, Applicants respectfully request that the Examiner clearly identify prior art that allegedly teaches the claimed features.

Hasebe describes an electronic data protection system for protecting electronic data from illegal copying by a third party. However, similarly to Hashimoto, Hasebe does not disclose or suggest "the encryption circuit being deactivated before the data control circuit receives the digital recording signal to be encrypted...wherein when the digital recording signal needs to be encrypted, the encryption circuit begins to start up and the digital recording signal is transmitted from the data control circuit to the memory to be stored in the memory during start-up of the encryption circuit, and when the encryption circuit becomes capable of operation, the digital recording signal stored in the memory is transmitted via the data control circuit to the encryption circuit and is encrypted by the encryption circuit to be recorded in the recording unit" as recited in claim 1.

For at least the reasons discussed with respect to claim 1, it is respectfully submitted that the Examiner fails to establish a *prima facie* case of obviousness in independent claims 2, 4, 7, 10 and 11.

Independent claim 2 as amended recites, *inter alia*, "the decryption circuit being deactivated before the data control circuit receives the digital recording signal to be decrypted...wherein when the digital recording signal encrypted and recorded on the recording medium needs to be decrypted and reproduced, during start-up of the decryption circuit, the digital recording signal having been stored before start-up of the decryption circuit is outputted via the data control circuit, and when the decryption circuit is capable of operation, the digital recording signal read by the reproducing unit is transmitted via the data control circuit to the decryption circuit and is decrypted by the decryption circuit to be outputted."

Independent claim 4 as amended recites, *inter alia*, "the encryption unit being deactivated before the determination unit determines that the digital signal needs to be encrypted...when the determination unit determines that the digital signal does not need to be encrypted, the digital signal is not encrypted by the encryption unit and the digital signal stored in the storage unit is outputted, and when the determination unit determines that the digital signal needs to be encrypted, the digital signal from a time of the determination to a time when the enabling of the encryption unit is completed by the encryption key is stored in the storage unit and is encrypted by the encryption circuit to be outputted after the enabling of the encryption unit is completed."

Independent claim 7 as amended recites, *inter alia*, "the decryption unit being deactivated before the determination unit determines that the digital signal needs to be decrypted...when the determination unit determines that the digital signal does not need to be decrypted, the digital signal is not decrypted by the decryption unit and the digital signal stored in the storage unit is outputted, and when the determination unit determines that the digital signal needs to be decrypted, the digital signal from a time of the determination to a time when the enabling of the decryption unit is completed by the encryption key is stored in the storage unit and is decrypted by the decryption circuit to be outputted after the enabling of the decryption unit is completed."

Independent claim 10 recites, *inter alia*, "wherein when the determination is that the digital signal does not need to be encrypted, the digital signal is not encrypted and the stored digital signal is outputted, and when the determination is that the digital signal needs to be encrypted, the digital signal from a time of the determination to a time when the function of encrypting is enabled is stored and is encrypted to be outputted after the enabling of the function of encrypting is completed."

Independent claim 11 recites, *inter alia*, "wherein when the determination is that the digital signal does not need to be decrypted, the digital signal is not decrypted and the stored digital signal is outputted, and when the determination is that the digital signal needs to be decrypted, the digital signal from a time of the determination to a time when the function of decrypting is enabled is stored and is decrypted to be outputted after the enabling of the function of decrypting is completed."

In view of the above remarks, it is respect fully submitted that Hashimoto and Hasebe, when taken alone or in combination (assuming they can be combined, which Applicant does not admit), does not make the present invention as claimed in claims 1, 2, 4, 7, 10 and 11 unpatentable. As claims 5, 6, 8 and 9 are dependent to claims 1, 4 and 7 respectively, it is respectfully submitted that these claims are also patentable for at least their dependency. Thus, it is further respectfully submitted that this rejection should be withdrawn.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Dennis P. Chen Reg. No. 61,767 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

By _____

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